**Lab Report: 1**



**Digital System Design Lab**

**Spring 2023**

**Submitted by:**

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**Semester: 6**

“On my honor, as a student of University of Engineering and Technology Peshawar, I have neither nor received unauthorized assistance on this academic work”

**Submitted to:**

**Eng:Muhammad Usman**

**Introduction to MODELSIM And Gate Level Modeling**

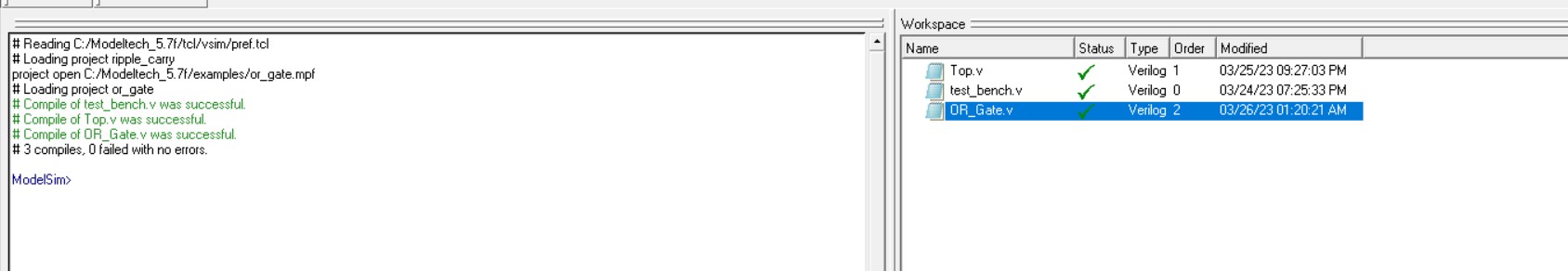
# Objective

Objectives of this lab are:

* To get familiar Modelsim
* To know about gate level modeling

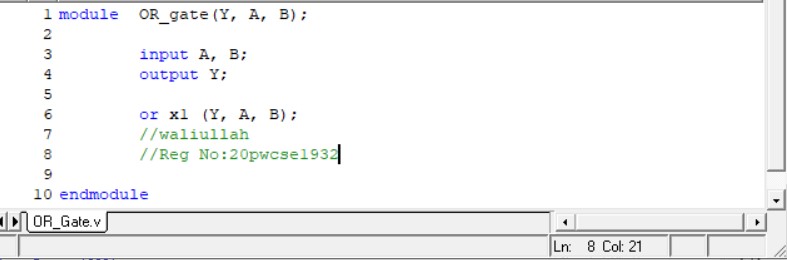
## MODELSIM

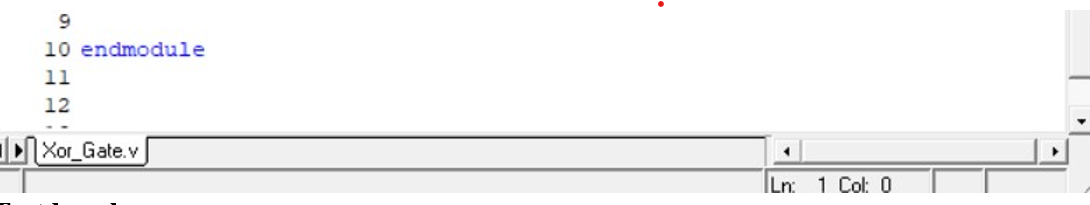
MODELSIM is a simulator which can be used for the simulations of both VHDL and Verilog HDL. It has the following interface.



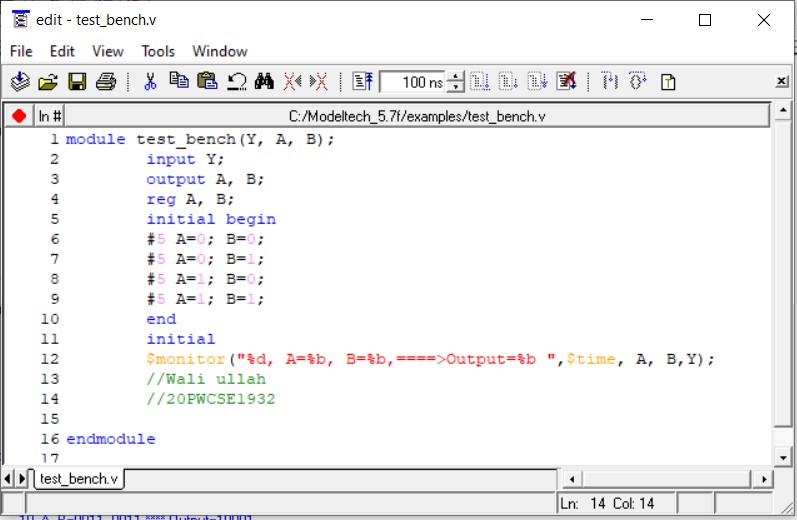
1. Implementation of OR Gate in MODELSIM

# Code

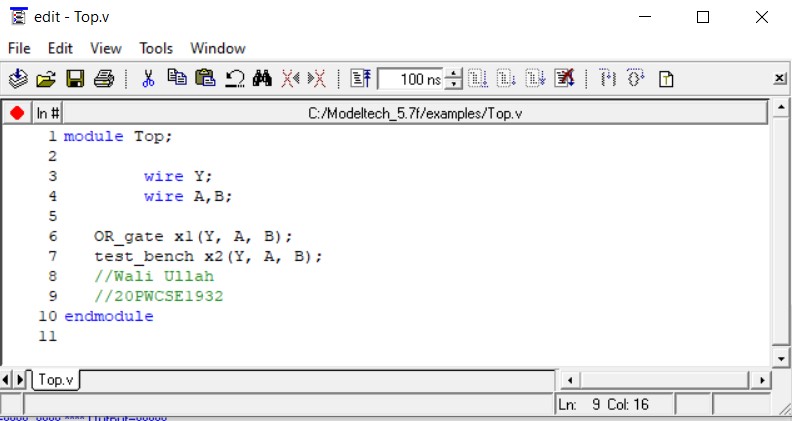


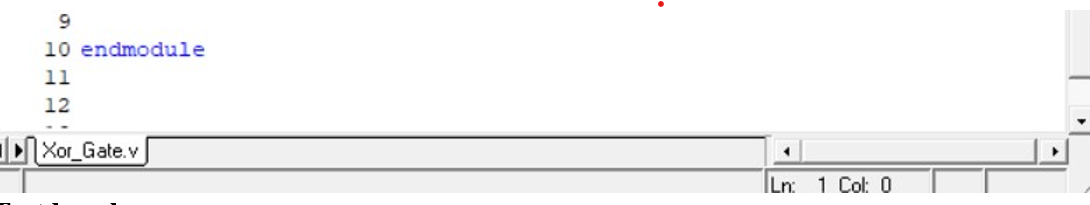


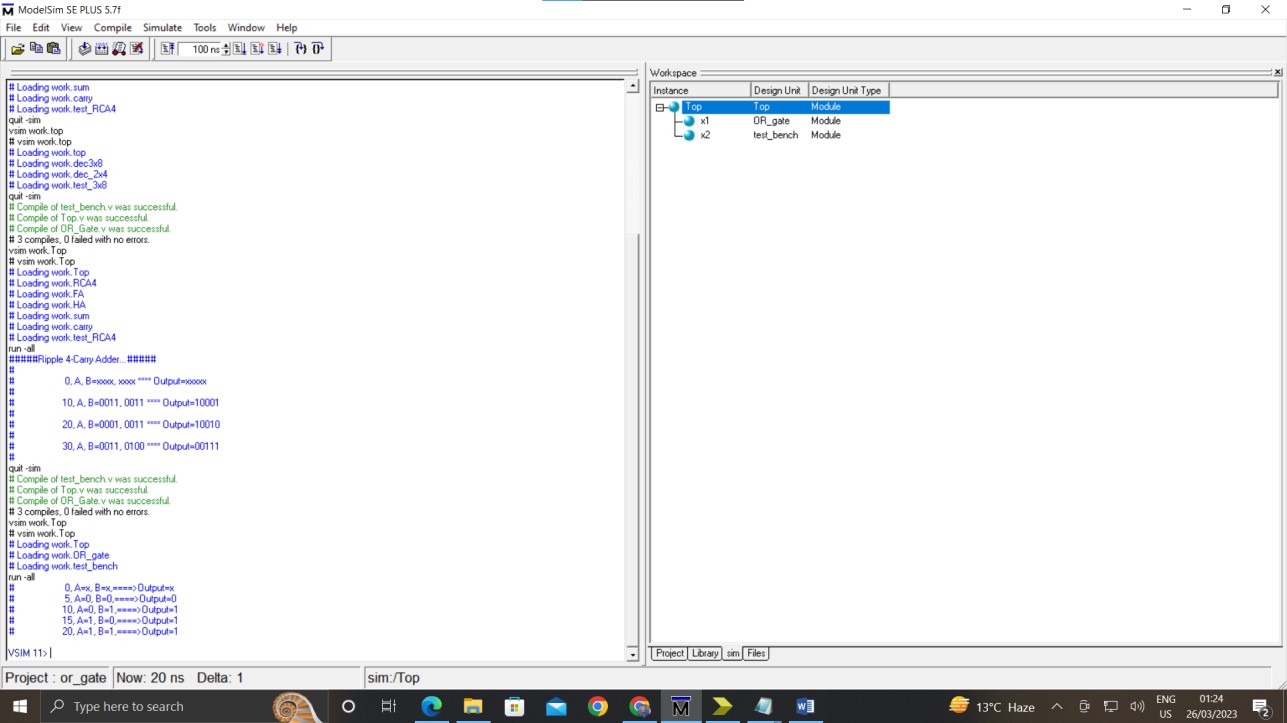
# Test bench



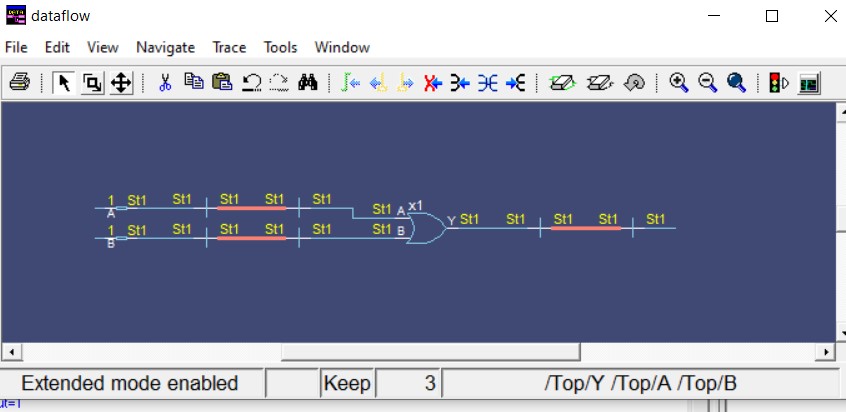
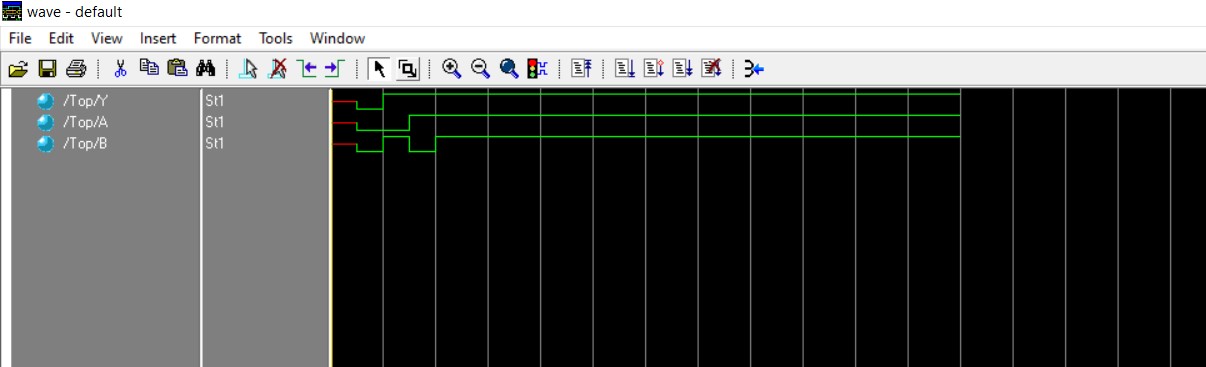
**Simulation Top:**



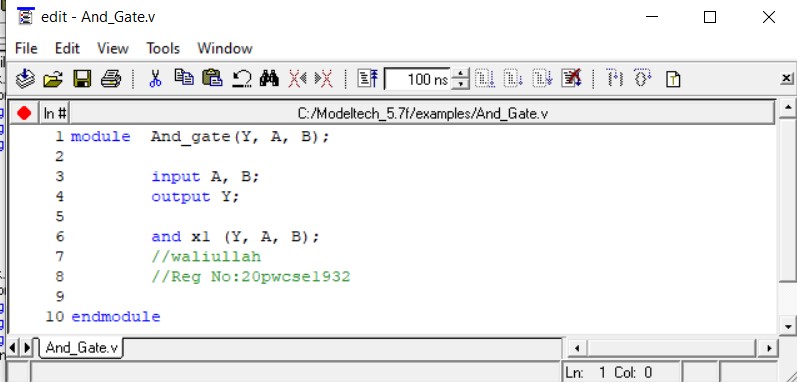


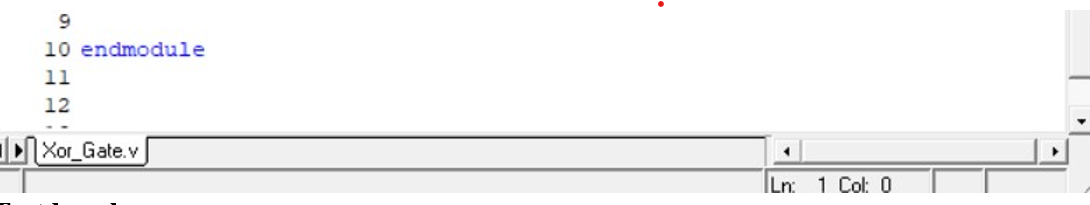


## Wave

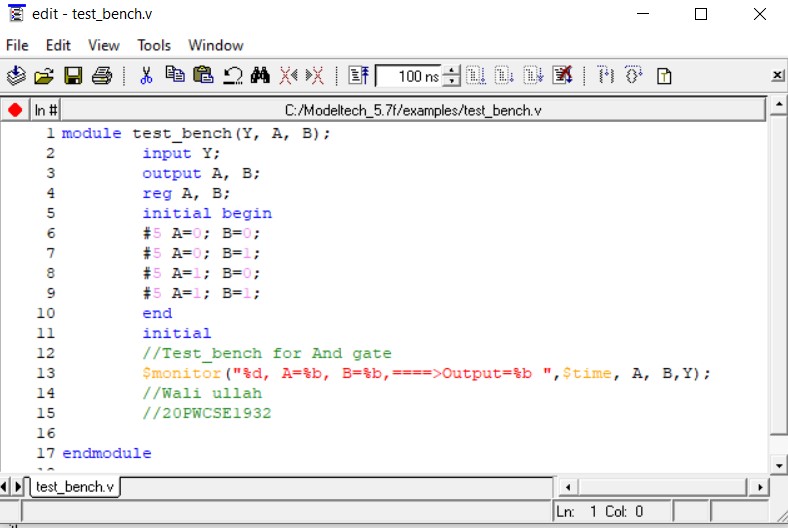


2. Implementation of And Gate in MODELSIM

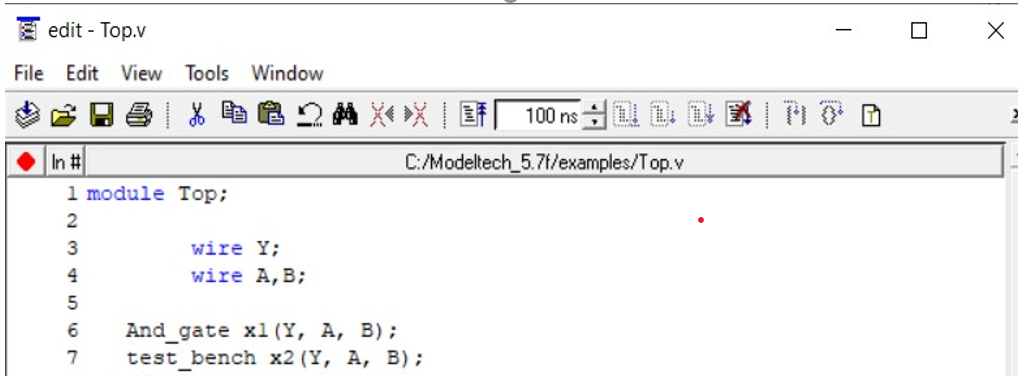


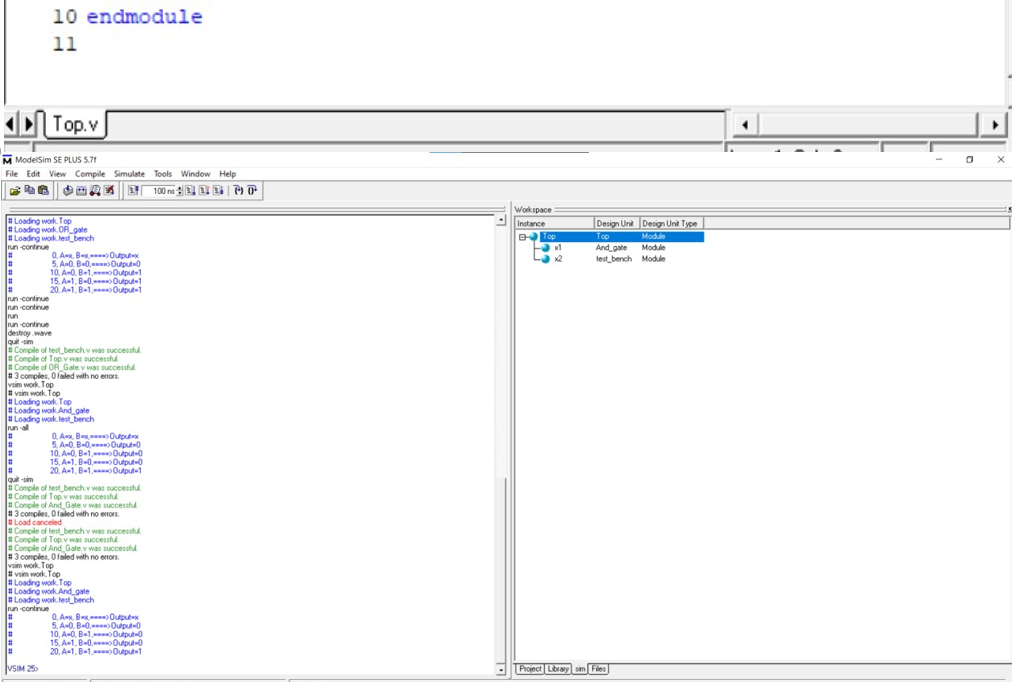


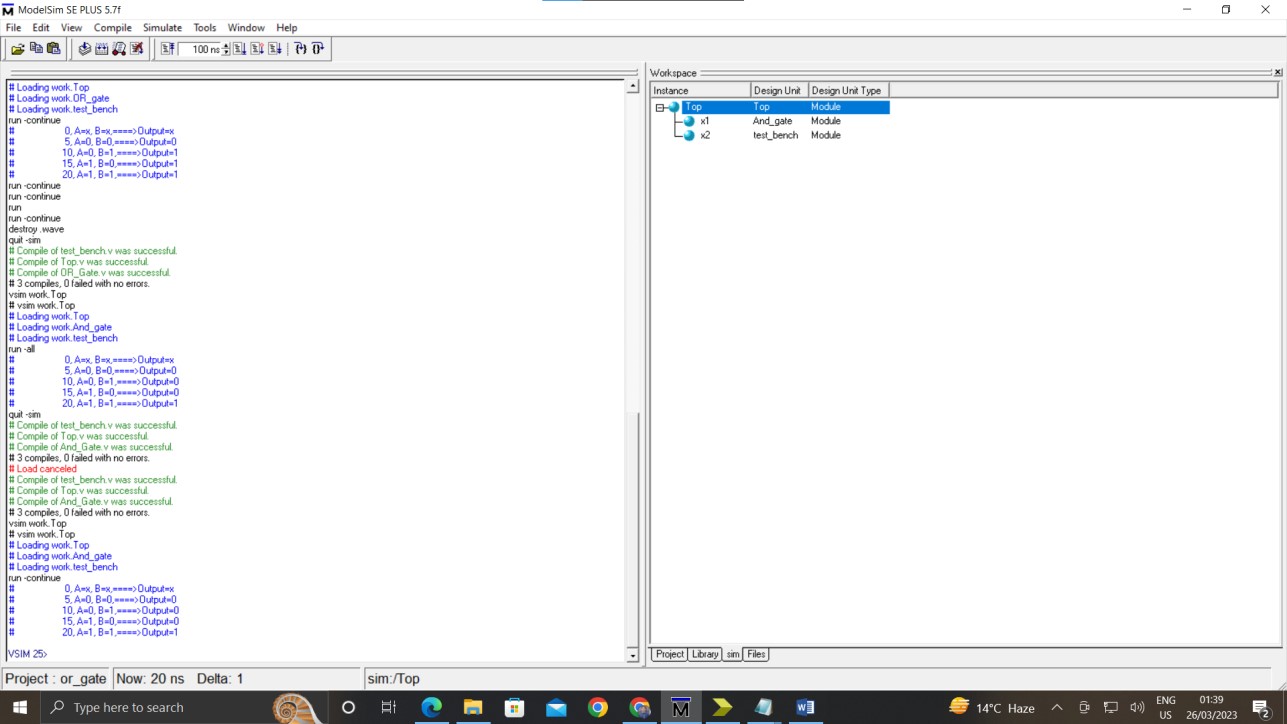
**Testbench:**



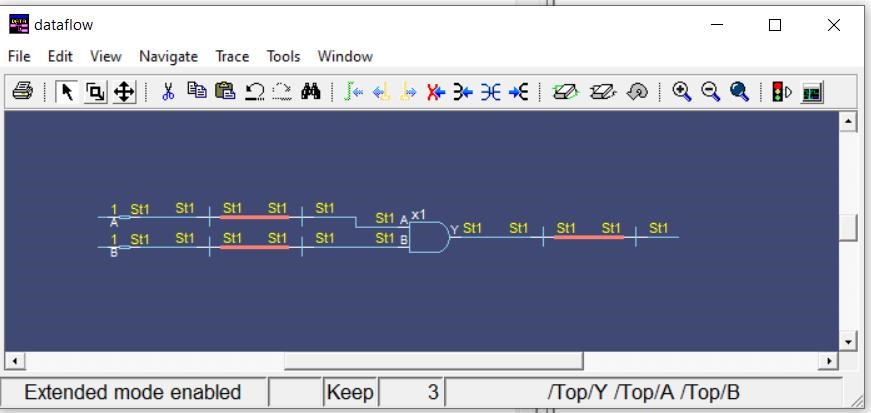
**Simulation Top:**





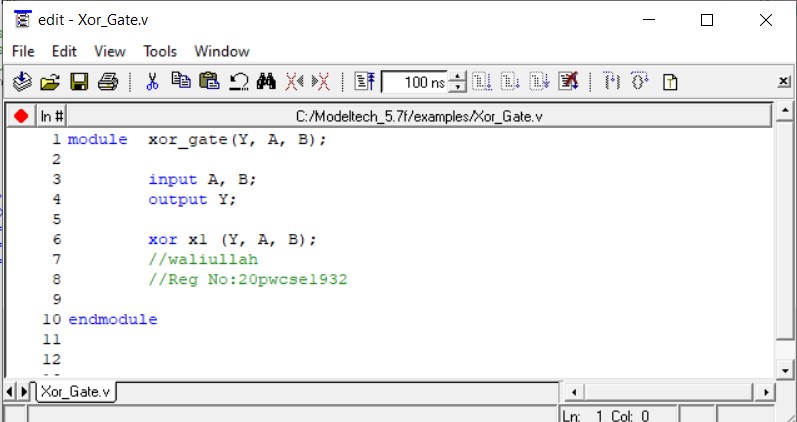


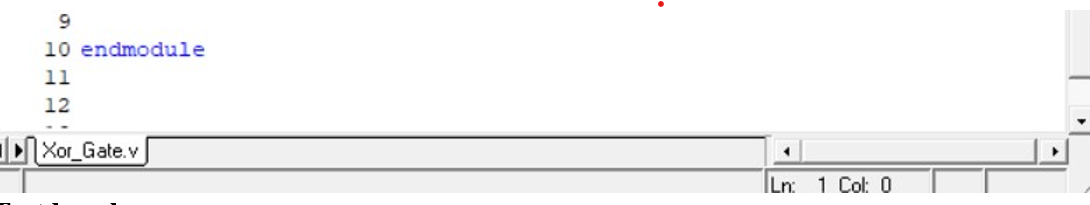
## Data Flow



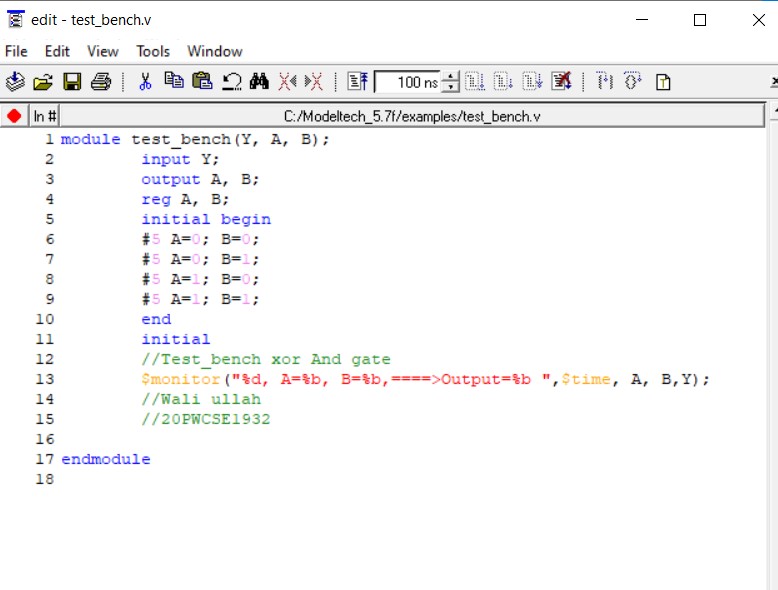
3. Implementation of XOR Gate in MODELSIM

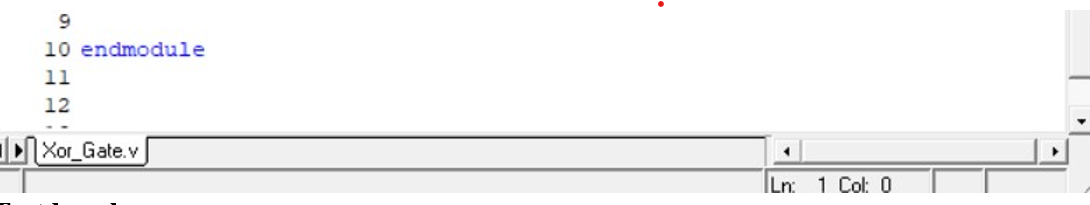
## Code



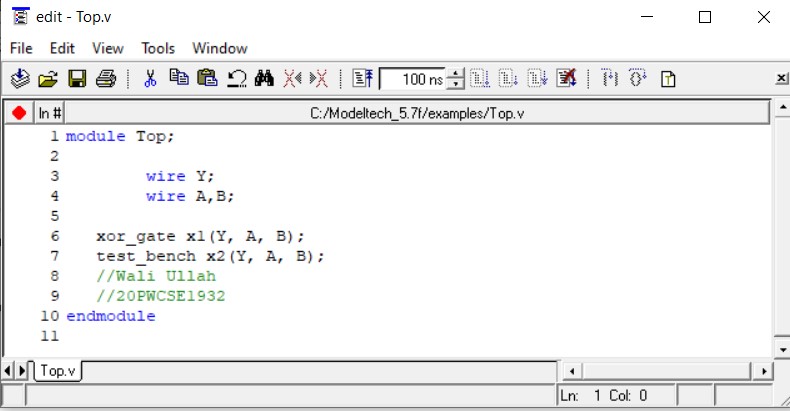


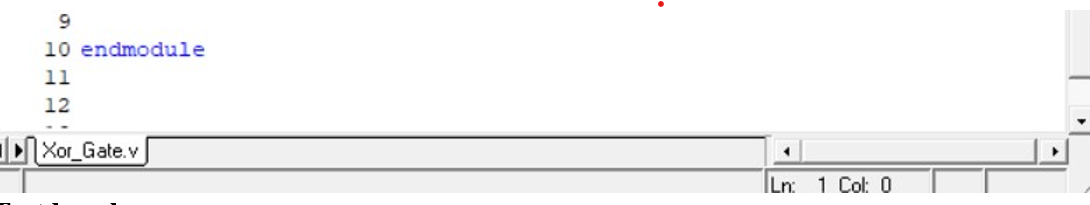
**Test bench**



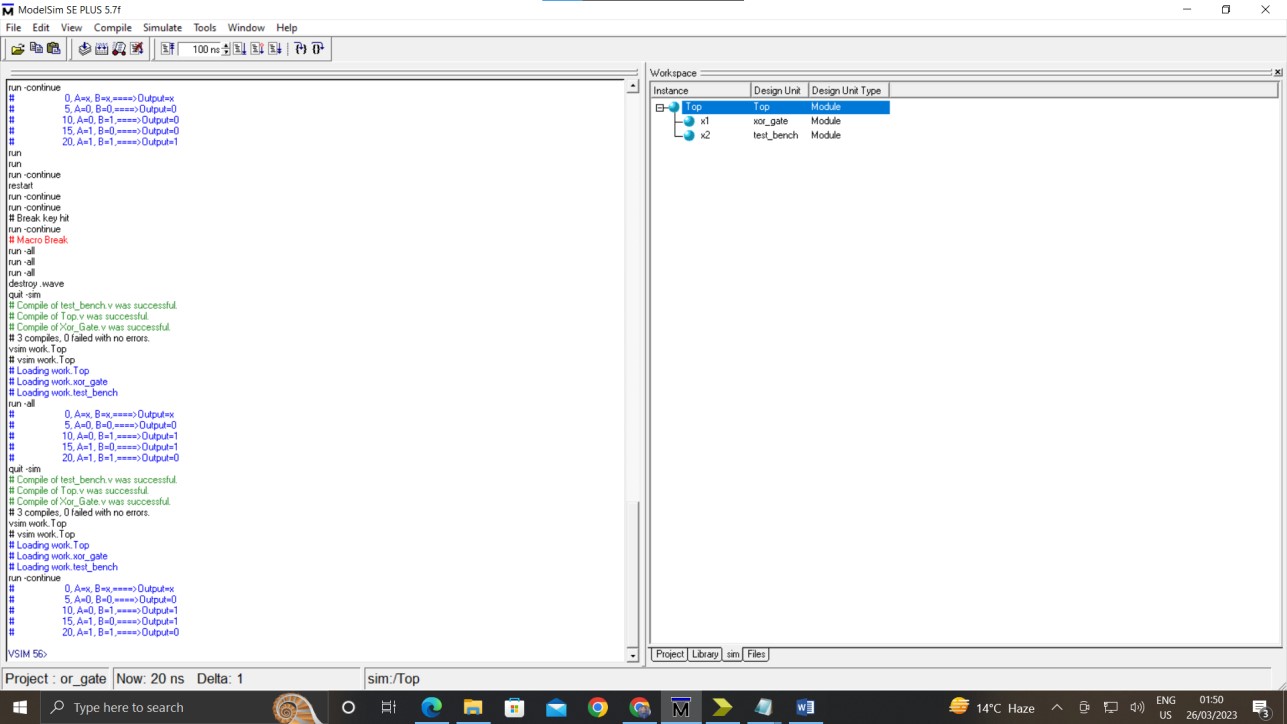


**Top**:

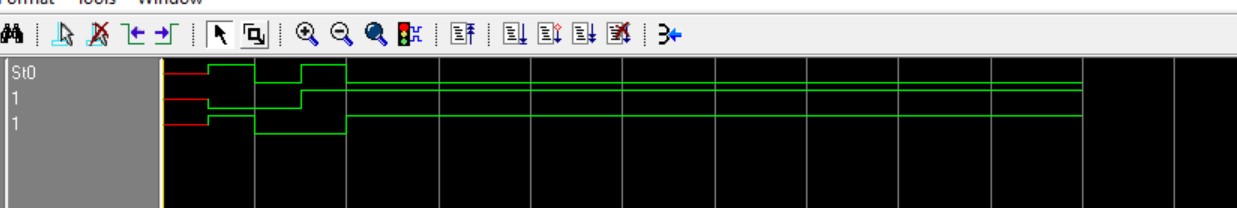




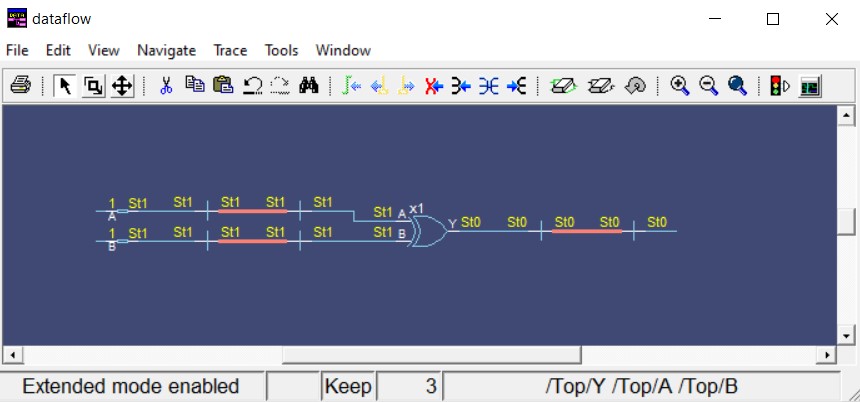
# Simulation



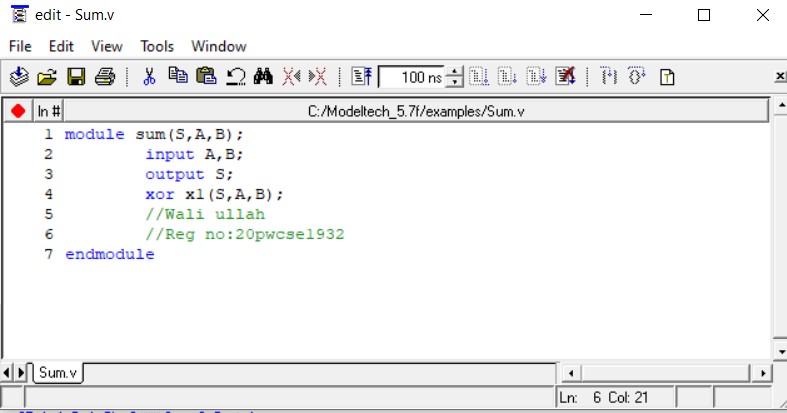
## Wave

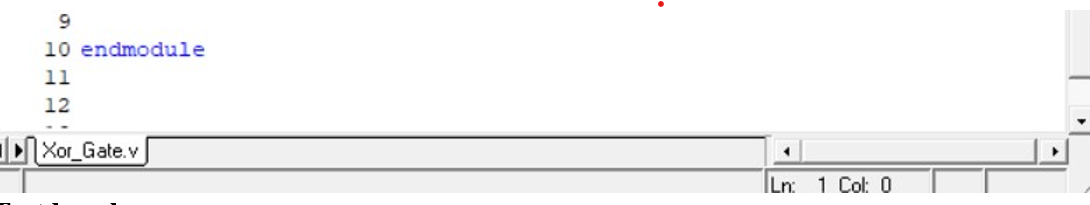


## Data Flow

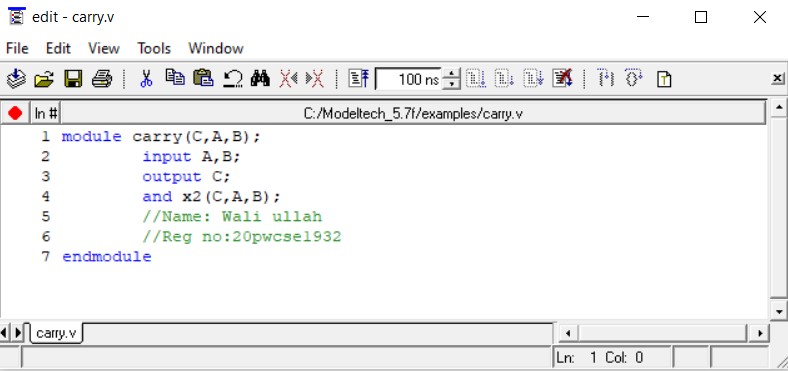


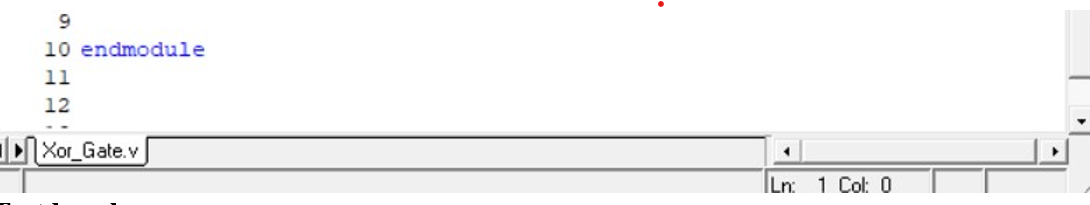
4. Implementation of Full Adder Using Two Half Adders in MODELSIM **Sum:**



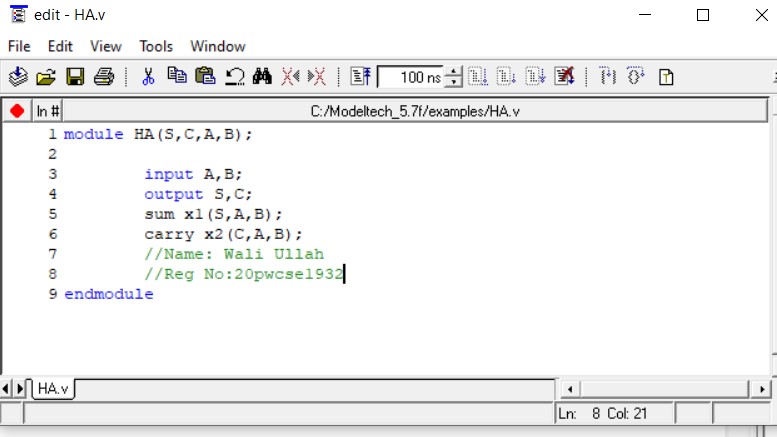


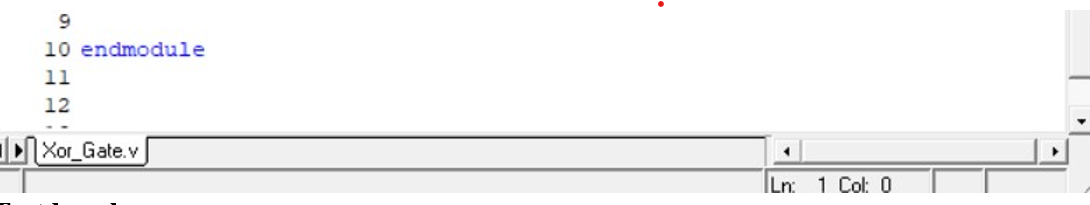
# Carry



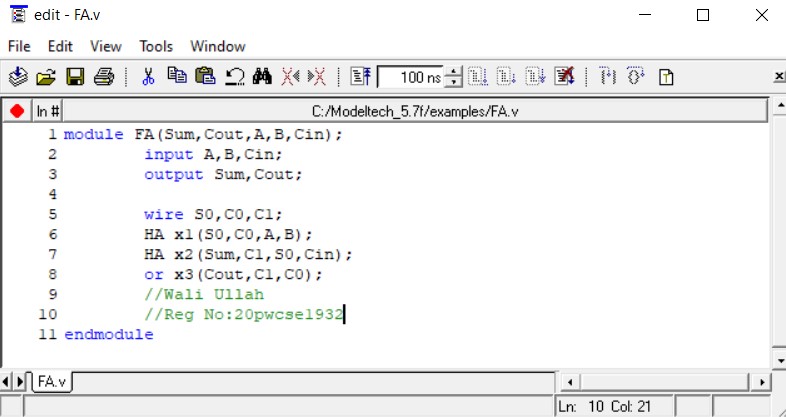


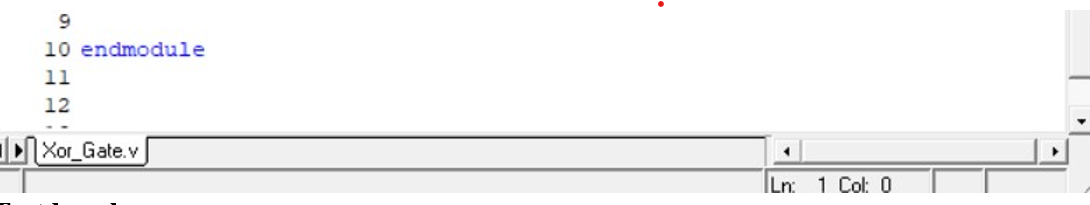
# Half Adder



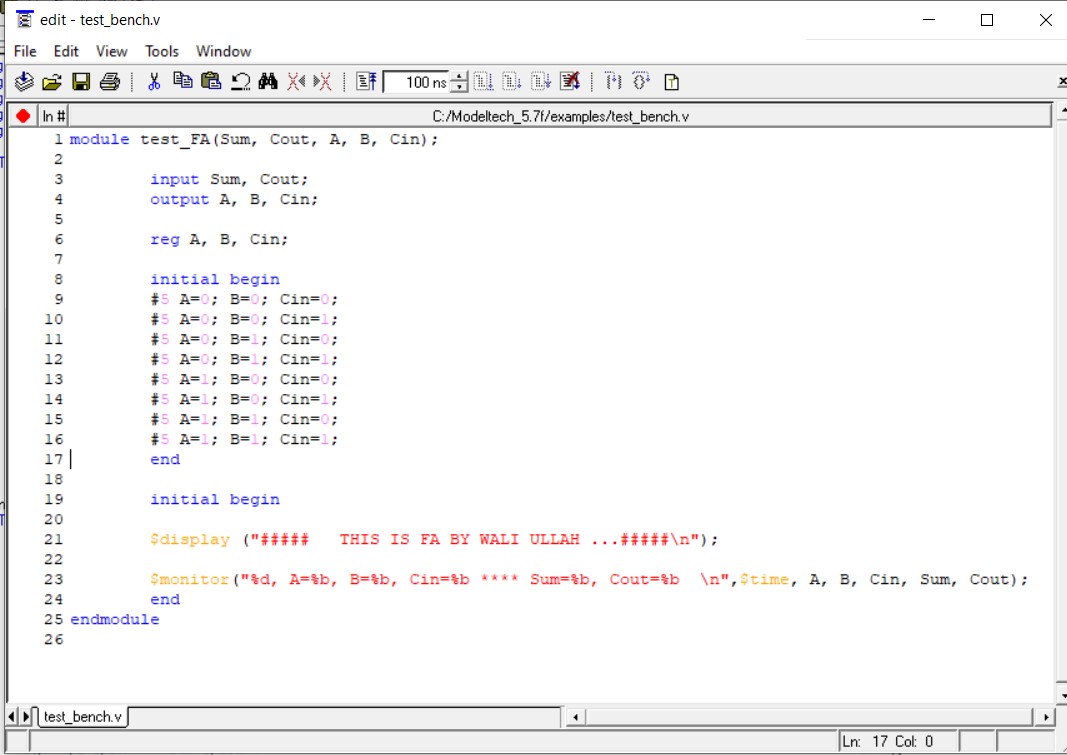


# Full Adder

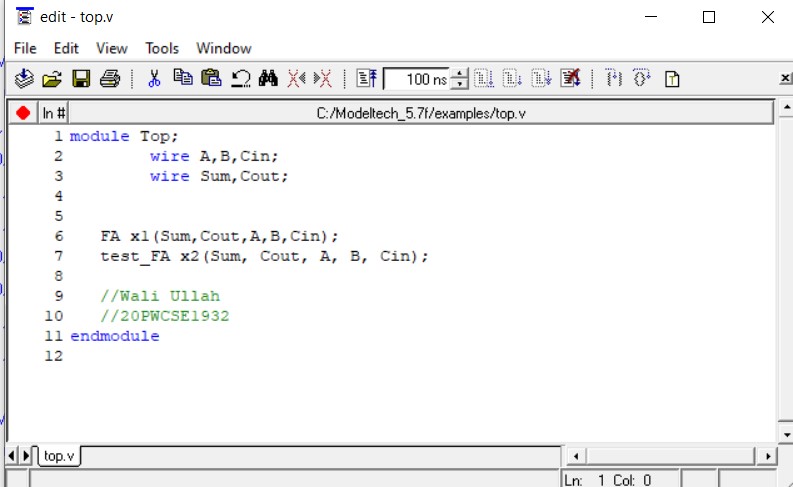


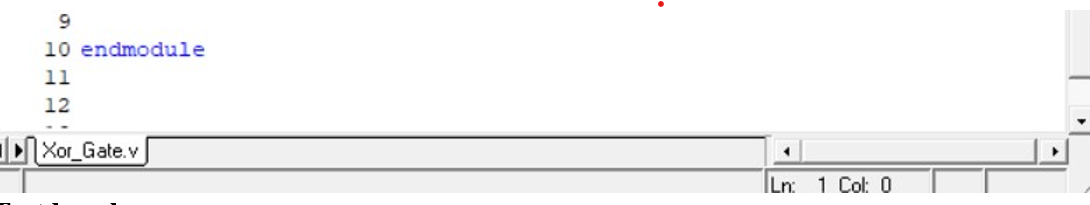


# Test bench

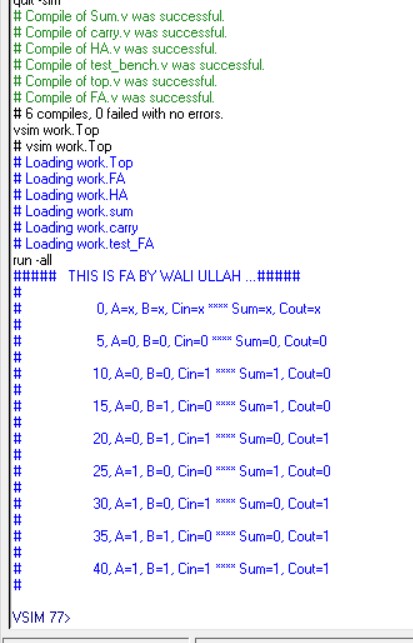


# Top

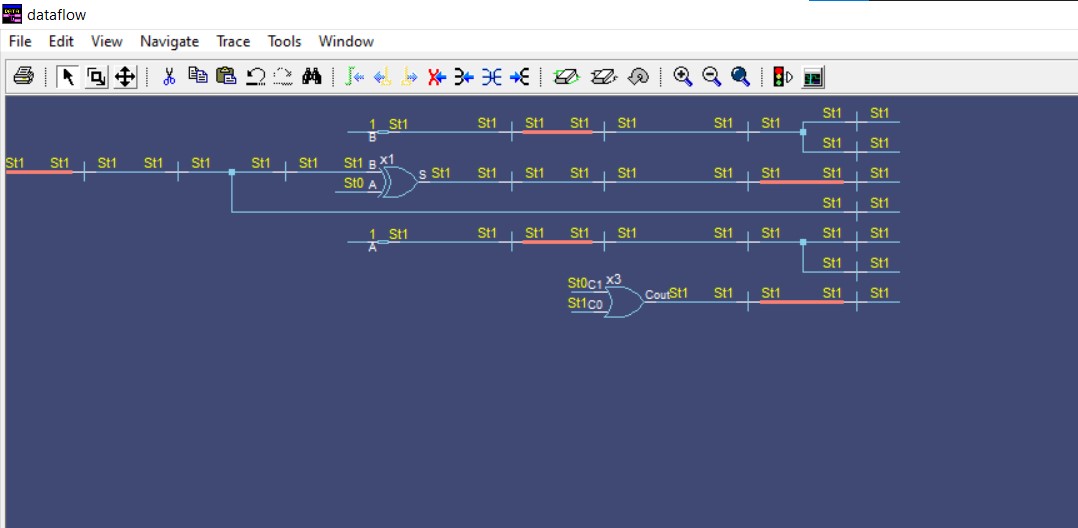




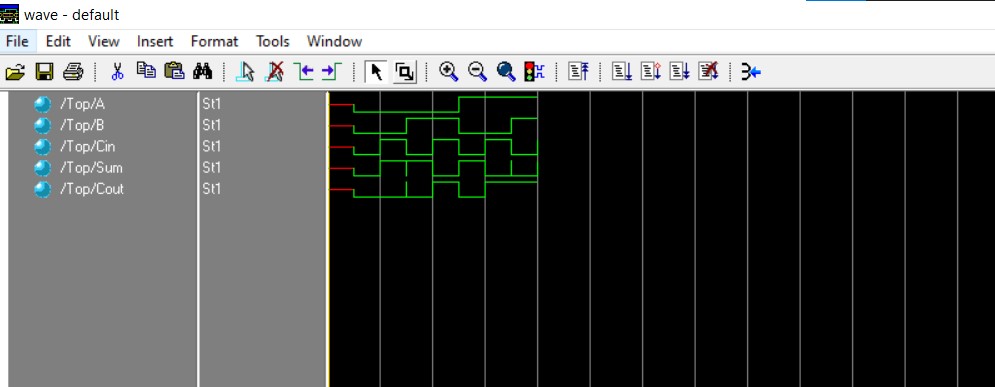
# Simulation



# Data Flow



**Wave:**

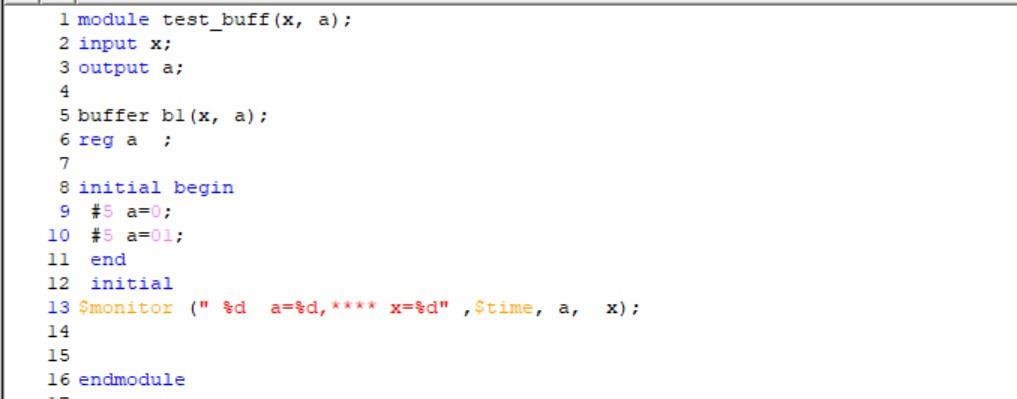


5. Implement a buffer at the gate level.

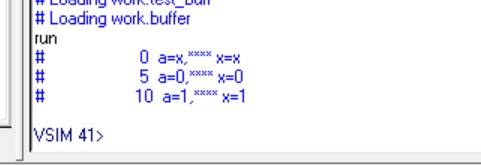
## Code



## Test bench



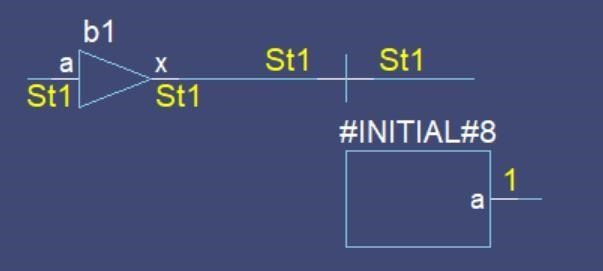
## Output



# Wave

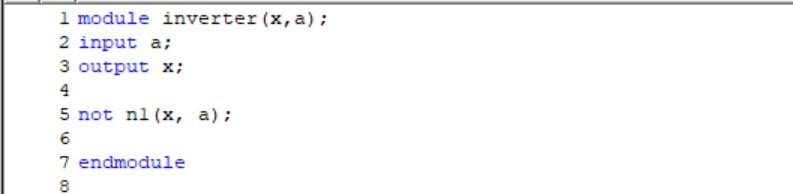


# Dataflow

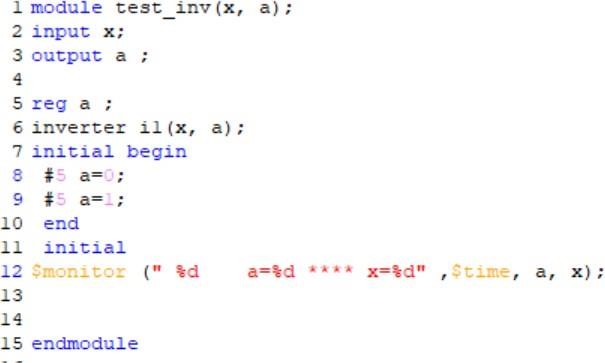


6. Implement an inverter at the gate level.

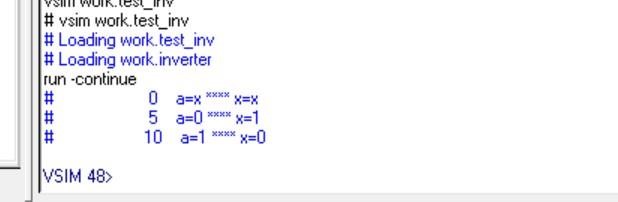
## Code



## Test bench



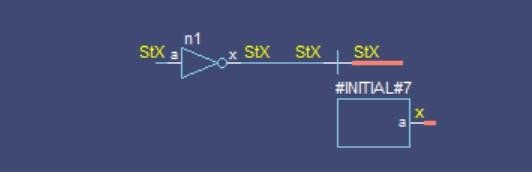
## Output



## Wave

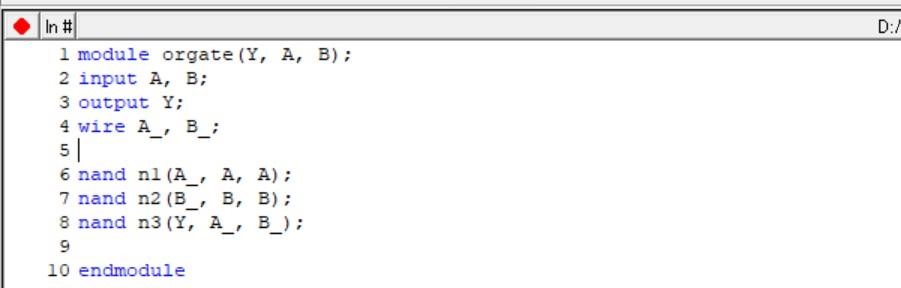


## Dataflow

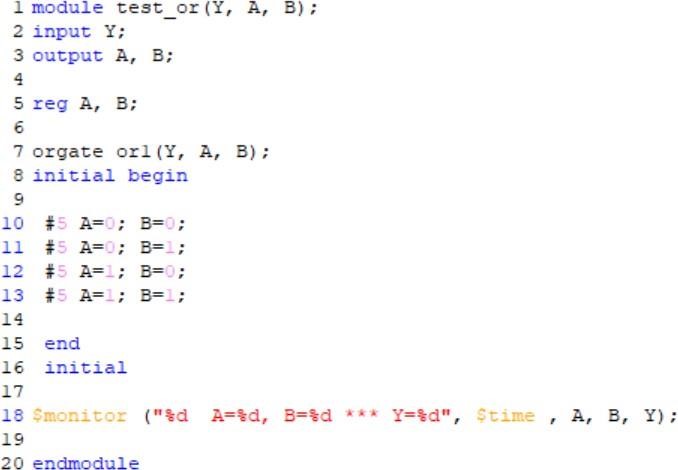


7. Implement an OR gate using a NAND gates.

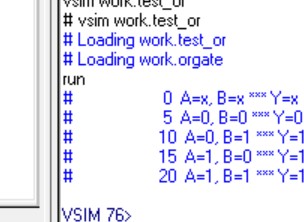
## Code



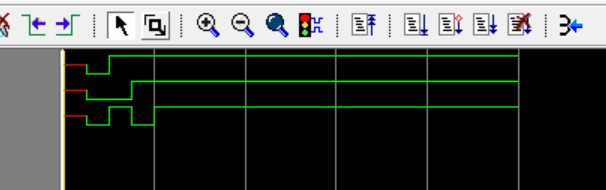
## Test bench



## Output



## Wave

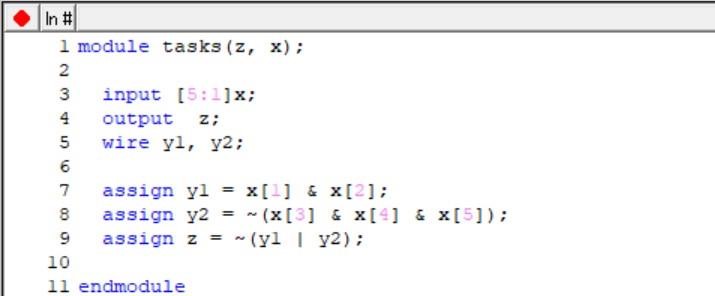


## Dataflow

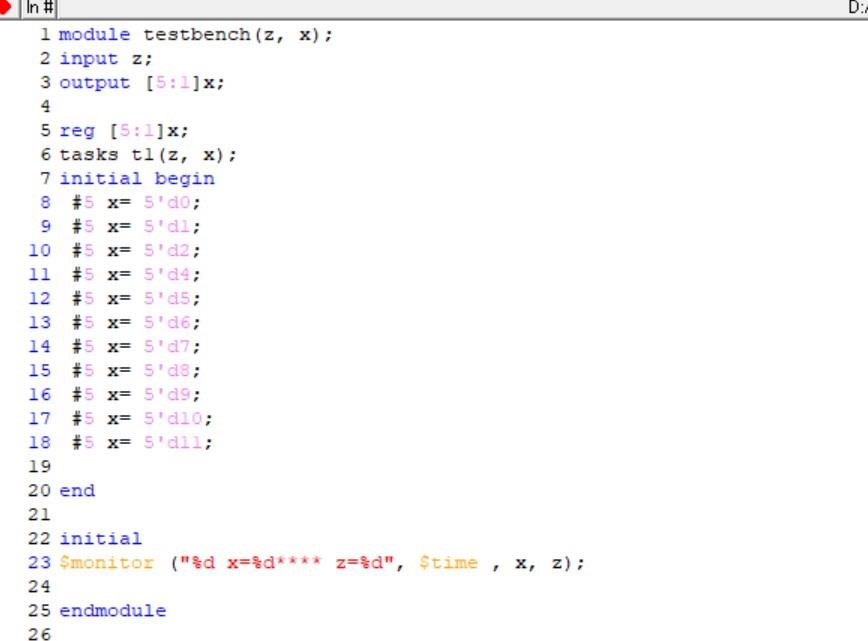
8. Implement the following equation where z is output and x1, x2, x3, x4, and x5 are inputs of the circuit. z = ( y1 + y2 )’ y1 = x1.x2

y2 = (x3.x4.x5)’

## Code



## Test bench



## Output

